

WHAT IS CLAIMED IS:

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- 1 1. A method of storing a texel in a texel cache comprising:
2 reading a t coordinate of the texel, the t coordinate comprising a plurality
3 of bits;
4 reading a s coordinate of the texel, the s coordinate comprising a plurality
5 of bits; and
6 forming an offset by concatenating bits of the t coordinate with bits of the
7 s coordinate.
 - 1 2. The method of claim 1 further comprising forming an index by
2 concatenating bits of the t coordinate with bits of the s coordinate.
 - 1 3. The method of claim 2 further comprising storing the texel in a
2 texel cache comprising a plurality of cache lines, wherein each cache line comprises a
3 plurality of storage elements.
 - 1 4. The method of claim 3 further comprising storing the texel in a
2 storage element identified by the offset.
 - 1 5. The method of claim 4 further comprising storing the texel in a
2 cache line identified by the index.
 - 1 6. The method of claim 5 wherein the forming an offset by
2 concatenating bits of the t coordinate with bits of the s coordinate is done by
3 concatenating the lower bits of the t coordinate with the lower order bits of the s
4 coordinate.
 - 1 7. The method of claim 6 further comprising retrieving the texel from
2 a main memory, wherein the texel has an address in main memory.
 - 1 8. The method of claim 7 further comprising forming a tag by
2 concatenating the high order bits of the s coordinate and high order bits of the t
3 coordinate, adding the address in main memory, and storing the tag in a look-up table.
 - 1 9. The method of claim 8 wherein the forming an index by
2 concatenating bits of the t coordinate with bits of the s coordinate is done by

3 concatenating middle order bits of the t coordinate with middle order bits of the s
4 coordinate.

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1 10. The method of claim 1 wherein the texel is associated with a
2 MIPmap having a level of detail comprising a plurality of bits, further comprising
3 forming an index signal by concatenating middle order bits of the s coordinate, middle
4 level bits of the t coordinate, and at least one bit of the level of detail.

1 11. The method of claim 1 wherein the texel is associated with a
2 texture having a texture identification comprising a plurality of bits, further comprising
3 forming an index signal by concatenating middle order bits of the s coordinate, middle
4 level bits of the t coordinate, and at least one bit of the texture identification.

1 12. The method of claim 1 wherein the texel is associated with a
2 texture having an r coordinate comprising at least one bit, further comprising forming an
3 index signal by concatenating middle order bits of the s coordinate, middle level bits of
4 the t coordinate, and at least one bit of the r coordinate.

1 13. The method of claim 1 wherein the texel has a main memory
2 address comprising a plurality of bits, further comprising forming an index signal by
3 concatenating middle order bits of the s coordinate, middle level bits of the t coordinate,
4 and at least one bit of the main memory address.

1 14. An integrated circuit comprising:
2 a texture cache subsystem for storing a texel;
3 a cache address generator subsystem for receiving an s and a t coordinate,
4 and for providing an index and offset to the texture cache subsystem; and
5 a graphics pipeline subsystem for providing the s and t coordinates to the
6 cache address generator subsystem, and memory addresses to the cache address generator
7 subsystem, and further for receiving a texel from the texture cache subsystem,
8 wherein the index and offset comprise bits of the s and t coordinates.

1 15. The integrated circuit of claim 14 wherein the index further
2 comprises at least one bit of a level of detail signal associated with the texel.

1 16. The integrated circuit of claim 14 wherein the index further
2 comprises at least one bit of a texture id associated with the texel.

1 17. The integrated circuit of claim 14 wherein the index further
2 comprises at least one bit of a memory address associated with the texel.

1 18. The integrated circuit of claim 14 wherein the index further
2 comprises at least one bit of an r coordinate associated with the texel.

1 19. A method of generating a texture cache address comprising:
2 reading an s coordinate of a texture, wherein the s coordinate comprises a
3 plurality of bits;
4 passing lower order bits of the s coordinate as a portion of an offset;
5 passing middle order bits of the s coordinate as a portion of an index; and
6 passing high order bits of the s coordinate as a portion of a tag.

1 20. The method of claim 19 further comprising:
2 reading a t coordinate of the texture, wherein the t coordinate comprises a
3 plurality of bits;
4 passing lower order bits of the t coordinate as a portion of an offset;
5 passing middle order bits of the t coordinate as a portion of an index; and
6 passing high order bits of the t coordinate as a portion of a tag.

1 21. The method of claim 20 further comprising reading a memory
2 address, and passing a portion of the memory address as a portion of the tag.

1 22. The method of claim 21 further comprising reading a level of detail
2 associated with the texel, and passing a portion of the level of detail as a portion of the
3 index.

23. The method of claim 21 further comprising reading a texture id associated with the texel, and passing a portion of the texture id as a portion of the index.

1 24. The method of claim 21 further comprising reading a memory
2 address associated with the texel, and passing a portion of the memory address as a
3 portion of the index.

1 25. The method of claim 21 further comprising reading an r coordinate
2 associated with the texel, and passing a portion of the r coordinate as a portion of the
3 index.

1 26. A method of storing address information for a group of texels
2 comprising:
3 storing an index and offset of a first texel; and
4 storing a line index of at least one of the other quad of texels,
5 wherein the stored address information comprises information necessary to
6 determine a group of addresses in a texture cache.

1 27. The method of claim 26 wherein the texture cache comprises a
2 plurality of cache lines, further comprising storing an indication of which cache lines
3 need to be updated.

1 28. The method of claim 27 further comprising storing information as
2 to the wrap mode used to store the group of texels in the texel cache.

1 29. A graphics processor comprising:
2 a graphics pipeline coupled to receive texels and provide s and t
3 coordinates and a memory address;
4 a cache address generator, coupled to receive the s and t coordinates and
5 the memory address, and configured to generate an offset, an index, and a tag using the s
6 and t coordinates and the memory address, and
7 a cache unit, coupled to provide texels, and receive the offset, index and
8 tag, wherein the cache unit further comprises a texture cache.

1 30. A computer system comprising:
2 a central processing unit (CPU);
3 a main memory coupled to the CPU; and
4 a graphics processor as set forth in claim 29, coupled to the CPU.

1 31. A graphics processor comprising:
2 a texture cache manager, coupled to receive texel addresses and provide a
3 packet of data, and a fetch request;

4 a memory controller coupled to receive the fetch request and provide a
5 cache line update;
6 a FIFO coupled to receive and provide packets, and configured to store a
7 plurality of packets; and
8 a texture cache controller coupled to receive data stored in cache lines,
9 wherein the packets comprise an offset of a first texel, an index of a first
10 texel, and information required to generate an offset and an index of a second texel.

1 32. A computer system comprising:
2 a central processing unit (CPU);
3 a main memory coupled to the CPU; and
4 a graphics processor as set forth in claim 31, coupled to the CPU.

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